REMARKS

Claims 1-38 are pending and each has been amended to conform to the requirements of U.S. patent practice. Favorable consideration in light of this preliminary amendment is respectfully requested.

Respectfully submitted,

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INTEGRATED READ-ONLY MEMORY, METHOD FOR OPERATING SAID READ-ONLY MEMORY AND PRODUCTION METHOD

~~Description~~

PRIORITY AND CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims the benefit of priority under 35 U.S.C. §§ 120, 365, and 371 to Patent Cooperation Treaty patent application no. PCT/EP03/01583, filed on February 7, 2003, which was published at WO 03/075350, in German.

[0002] This application is further related to and claims the benefit of priority of February 21, 2002 under 35 U.S.C. § 119 to German patent application no. DE 102 07 300.7, filed on February 21, 2002.

BACKGROUND OF THE INVENTION

1. Technical Field.

[0003] The invention relates to an integrated read-only memory, a method for operating said read-only memory and a method for producing an integrated read-only memory.

2. Related Art.

[0004] As the integration density in microelectronics increases, the demand for large-scale integrated read-only memories is also increasing. These memories are used for example for on-chip storage of audio, graphics or video data.

[0005] Read-only memories are distinguished by the fact that the memory content is preserved even when the operating voltage is switched off. Such read-only memories are, in particular, also of programmable design (PROM). Programmable components therefor are for instance fuses, diodes or, alternatively, special MOSFETs having an additional so-called floating gate. The latter is charged during programming and thereby shifts the threshold

voltage of the MOSFET. Since the floating gate is insulated all around with SiO_2, the charge retention can be guaranteed for approximately ten years.

[0006] Over and above the programming function, there are read-only memory variants which are of erasable design (EPROM, EEPROM). The memory content can be erased by means of ultraviolet light in the case of EPROMs; the erase function is effected electrically in the case of EEPROMs.

[0007] Flash memories constitute a particular embodiment of erasable read-only memories. They are electrically erasable, in which case, rather than being able to erase the individual memory cells separately, it is only possible to erase a whole block on the chip at once. In this case, the erasure is effected by means of a single erase pulse that lasts a few seconds. The advantage in this case is that the memory chip, for erasure, does not have to be demounted and placed into an erase device.

[0008] Integrated memories are usually constructed in the form of arrays. So-called selection transistors are used to select individual memory elements, so that their content can be read out. Individual selection transistors are selected via word lines. In this case, the word lines are connected to the control electrodes of selection transistors. The memory content is read out via bit lines. Writing to or configuring memory cells usually requires additional lines for accessing the memory element. This enlarges the construction of integrated read-only memories and makes them more complicated to handle.

[0009] An article by C.P. Collier et al., *Electronically Configurable Molecular-Based Logic Gates*, Science, Volume 285, p. 391, 1999 ~~[1]~~ discloses an electronically configurable connection having a molecular monolayer between two contacts produced lithographically. In this case, the contacts are formed as Al-Ti electrodes. Rotaxane molecules are used as the molecular layer.

[0010] The electrical behavior of this connection can be described as follows: if a layer is negatively polarized, then the current at the connection rises with increasing negative polarity. Such a treatment of the electrical connection changes the switching behavior to the effect that now only a current

that is lower by a factor of 60 to 80 is measurable in the case of a negatively polarized layer than without the prior treatment of the connection with a positively polarized layer.

[0011] The connection may thus be understood as a switch which may have an open state (poorer conductivity) and also a closed state (better conductivity). The open state permits a current flow at negative voltage on account of a resonance tunnel effect in the rotaxane-electrode junction. The switch's transition from the open state to the closed state through application of a sufficient positive voltage is irreversible, with the result that a switch, once closed, can no longer assume an open state.

[0012] The connection is disclosed for use in logic circuits.

[0013] A further electronically configurable switch is disclosed in C.P. Collier et al., *A [2]Catenane-Based Solid State Electronically Reconfigurable Switch*, Science, Volume 289, p. 1172, 2000~~[2]~~: the electrodes used are a polycrystalline silicon electrode, on the one hand, and a metal electrode, on the other hand. A molecular monolayer between the electrodes contains ~~[2]~~ Catenane.

[0014] Operation of the switch exploits the effect that mechanically blocked, intermeshing molecular rings of the ~~[2]~~ catenane are shifted relative to one another upon oxidation and subsequent reduction and the electrical properties of the switching connection are thereby changed. This voltage-controlled shift is reversible. The configuration is thus effected along a hysteresis loop. Depending on the previously applied configuration voltage, it is possible to observe a specific switching behavior upon application of a predetermined read voltage.

[0015] A further embodiment of a molecularly constructed switch is revealed in D.I. Gittins et al., *A Nanometre-Scale Electronic Switch Consisting of a Metal Cluster and Redox-Addressable Groups*, *Nature*, Volume 408, p. 67, 2000~~[3]~~. Here, too, the electron transport is controlled by means of molecular paths. A bipyridinium compound is used as the molecular layer.

[0016] A metal-insulator-metal arrangement is proposed in A. Beck et al., *Reproducible Switching Effect in Thin Oxide Films for Memory Applications*, Applied Physics Letters, Volume 77, p. 139, 2000~~[5]~~. An insulator oxide, for instance $SrZrO_3$ or $SrTiO_3$ or $Ca_2Nb_2O_7$, is applied as an epitaxial or polycrystalline film onto an $SrRuO_3$ film or a Pt film as electrode. The top electrode made of Au or Pt is applied onto the insulator via a Ti layer.

[0017] A read access to the switching arrangement is effected in a voltage range of -0.5 Volt to +0.5 Volt in the case of $SrZrO_3$ as insulator doped with 0.2 Cr. The current/voltage relationship is approximately linear in this read voltage range. The current flow over this voltage range depends on the previous configuration of the insulator. The insulator is configured by application of voltages of +1 Volt or -1 Volt over a duration of 2 ms. Through application of the negative configuration voltage, the insulator flips into its low-impedance state and in this case has a resistance characteristic curve that differs significantly from the resistance characteristic curve after application of the positive configuration voltage. Through application of the positive configuration voltage, the insulator flips into its high-impedance state. The configuration is reversible.

[0018] The change in the resistance characteristic curves that is brought about by configuration voltage pulses is caused by a change between amorphous and crystalline insulator states.

[0019] G. Wicker et al., Nonvolatile, High Density, High Performance Phase Change Memory, www.Ovonyx.com ~~[4]~~ reveals chalcogenide alloys that are configured by controlled heating and cooling. In this case, the application of a voltage pulse brings about a change between amorphous and crystalline states, and vice versa.

[0020] H.J. Gao et al., Reversible, Nanometer-Scale Conductance Transitions in an Organic ...", Physical Review Letters, Volume 84, No. 8, p. 1780, 2000 ~~[6]~~ uses a complex comprising 3-nitrobenzal malonitrile and 1,4-phenylenediamine as a layer whose conductivity can be changed on account of a change between crystalline and amorphous states.

[0021] US Patent No. 4,590,589 ~~[7]~~ discloses an electrically programmable read-only memory having voltage-programmable structures produced in finished fashion, for the provision of predictable and selectable programming voltages.

BRIEF SUMMARY

[0022] The invention ~~is based on the problem of specifying~~ relates to an integrated read-only memory which has a high integration density and can be programmed in a small number of steps.

[0023] Furthermore, the invention ~~is based on the object of specifying~~ relates to a method for producing such an integrated read-only memory.

[0024] ~~The objects are achieved by means of the~~ An embodiment of an integrated read-only memory ~~according to the features of claim 1~~ may have selection transistors each having a drain connection, an electrode for feeding a voltage or a current, a layer between the drain connections and the electrode, the electrical resistance of which can be changed through the effect of a configuration voltage or a configuration current, a source connection per selection transistor, a bit line that is electrically connected to at least one source connection, in which the layer is formed as a common layer for linking the drain connections to the electrode, and the electrical resistance of the layer can be changed locally.

[0025] , An embodiment of an ~~the~~ operating method ~~according to the features of claim 24~~ may include producing an array of selection transistors using CMOS technology, leadin drain contacts of the selection transistors to the surface of the arrangement, depositing a layer whose electrical resistance can be changed through the effect of a configuration voltage or a configuration current, it being possible for the electrical resistance of the layer to be changed locally, arranging an electrode above the layer, forming a source connection per selection transistor, forming a bit line which is electrically connected to at least one source connection, where the layer is deposited as a common layer for linking the drain connections to the electrode.

[0026] An embodiment of the method may also included~~and also the production method according to the features of claim 25~~ depositing a layer as a common layer for linking the drain connections to the electrode above the selection transistors.

[0027] The foregoing discussion of the summary is provided only by way of introduction. Other systems, methods, processes, apparatuses, features and advantages of the invention will be, or will become, apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] This invention can be better understood with reference to the following drawings and description. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. Moreover, in the figures, like referenced numerals designate corresponding parts throughout the different views.

Figure 1 shows a cross section through part of an integrated read-only memory in accordance with a first exemplary embodiment of the invention using planar selection transistors;

Figure 2 shows a cross section through part of an integrated read-only memory in accordance with a first exemplary embodiment of the invention using vertical selection transistors; and

Figure 3 shows a perspective view with elements illustrated partly in exploded fashion in a detail from a read-only memory according to Figure 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] Exemplary embodiments of the invention are illustrated in the drawings and explained in more detail in the description below. Identical elements are identified by the same reference symbols throughout the figures.

[0030] The read-only memory according to the invention ~~contains~~ may include selection transistors each having a drain connection and also an electrode for feeding a voltage or a current. A layer is provided between the drain connections and the electrode. The electrical resistance of the layer can be changed through the effect of a configuration voltage or a configuration current.

[0031] Thus, the use of a layer whose electrical resistance or whose electrical conductivity can be changed by electrical configuration is proposed. Through the effect of a configuration current or a configuration voltage, the electrical property of "resistance" or "conductivity" of the layer is set, so that the setting can be interrogated in a read step.

[0032] ~~What is essential in this case is that switching~~ Switching elements of the integrated read-only memory thus formed need only have two connections, more precisely the electrode connection and the connection to the drain of the respective selection transistor. Via these two connections, the intervening layer used as memory element can both be configured – also used as a synonym for "written to" or "programmed" – by suitable application of voltage or current and its content – represented by a specific layer state – can be read out. Configuration connection and read connection no longer have to be provided separately from one another.

[0033] ~~Precisely this~~ This measure ~~enables~~ may allow the integration density to be considerably increased. Since each memory cell can be driven individually, the driving can be effected at high speeds. Moreover, the selection of suitable material systems makes it possible to use low operating voltages, at least lower operating voltages than in the case of conventional flash memory technologies.

[0034] When a memory cell's selection transistor is driven via the gate, the content is read out via a bit line connected to the source. The current flow from the electrode via the electrically switchable layer and the drain-source path of the selection transistor to the bit line is a measure of the content of the memory

cell. In this case the current flow is significantly influenced by the preset state of the layer, more precisely its resistance characteristic.

[0035] Such a memory cell can be programmed by selection of the corresponding selection transistor and subsequent application of a configuration voltage between electrode and bit line, or, alternatively, by variation in the gate driving of the selection transistor with a voltage applied to the electrode. If the programming is irreversible, it is possible to realize a one-time programmable memory, and a read-only memory that can be written to many times can be realized if the state change is reversible.

[0036] Preferably, the layer is formed as a common layer for linking the drain connections, and in particular all the drain connections, to the electrode. Consequently, only a single electrically switchable layer ~~is~~ may be provided, to which a plurality or even all of the drain connections of selection transistors are connected, that is to say are electrically conductively connected thereto. In this advantageous development of the invention, it is assumed that the common layer can be changed locally in terms of its electrical properties and is thus programmable. Thus, individual delimitable local regions of the layer may have differing conductivity. Precisely such a region then forms a memory cell to which a selection transistor is connected. The electrode is preferably formed as a common electrode above said layer.

[0037] This significantly simplifies the production process but also significantly increases the integration density.

[0038] Preferably, the resistance of the layer can be switched over.

[0039] This development of the invention aims for the best possible discrimination between the conductivity values of the layer states that can be set.

[0040] Preferably, the resistance of the layer can be switched over between two resistance characteristic curves. It is assumed in this case that, in the read operation, the resistance is not constant over a read voltage range that can be

applied, but rather follows a characteristic curve. In this case the characteristic curves assigned to the layer states are intended to be well discriminatable.

[0041] The read operation of the memory cell is distinguished by a read voltage applied to the layer or a read current fed to the layer within a defined voltage or current range. In contrast thereto, the configuration operation may have a configuration voltage or a configuration current preferably outside the voltage or current range provided for read operation.

[0042] In this case, configuration and read operation can be effected in completely different voltage or current bands and incorrect operation can thus be avoided.

[0043] Preferably, the integrated read-only memory is designed as a flash memory. In this case, by the application for example of a configuration voltage to the electrode and simultaneous activation of all the selection transistors, it is possible for all of the local memory areas of the electrically switchable layer to be put into the same state with regard to the conductivity.

[0044] A fast erasure of the memory content is thus possible.

[0045] The bit lines connected to source connections of the selection transistors may be connected to a decoder circuit. For this purpose, the bit line may be formed in particular in a manner accessible for an external connection.

[0046] Each gate connection of a selection transistor may be electrically connected to a word line.

[0047] The word line, for its part, may be connected to a decoder circuit. In this case, the word line may, in particular, be accessible for an external connection.

[0048] These embodiments serve for the selection of selection transistors in multiplex operation with decoders that determine the addresses being connected upstream.

[0049] The selection transistors are arranged on the substrate preferably in an array.

[0050] In this case, the selection transistors may have a planar construction in the substrate.

[0051] By virtue of the planar construction, an integration density that is increased somewhat compared with the vertical construction of the transistors is accepted in favor of simplified production steps. The integration density of a memory cell in the case of a planar arrangement of the selection transistors amounts for example to approximately $6*F^2$ or $8*F^2$, where F is the minimum feature size.

[0052] In the case of a vertical construction of the selection transistors in the substrate, the integration density of a memory cell amounts to approximately $4*F^2$, where F is the minimum feature size.

[0053] Preferably, the electrically switchable layer is formed as a molecular layer, and in particular is formed as a monolayer as is known in the art. The layer may include rotaxane, catenane, and/or a bispyridinium compound, and the like or any combination thereof. For example, the monolayer may be formed as described in C.P. Collier et al., *Electronically Configurable Molecular-Based Logic Gates*, Science, Volume 285, p. 391, 1999; C.P. Collier et al., *A [2]Catenane-Based Solid State Electronically Reconfigurable Switch*, *Science*, Volume 289, p. 1172, 2000; and/or D.I. Gittins et al., *A Nanometre-Scale Electronic Switch Consisting of a Metal Cluster and Redox-Addressable Groups*, *Nature*, Volume 408, p. 67, 2000; each of which is incorporated by reference herein in their entirety.

~~In this case, it may contain rotaxane, in particular. The explanations in [1] with regard to the chemical composition of the layer, the electrode formation and linking and also the operation of the layer shall be disclosed herewith as being associated with the invention.~~

~~However, the layer may also contain catenane. The explanations in [2] with regard to the chemical composition of the layer, the electrode formation and linking and also the operation of the layer shall be disclosed herewith as being associated with the invention.~~

~~The layer may also contain a bispyridinium compound. The explanations in [3] with regard to the chemical composition of the layer, the electrode formation and linking and also the operation of the layer shall be disclosed herewith as being associated with the invention.~~

[0054] The layer may also be formed as a dielectric, using an oxide component, as is known in the art. The layer may include $SrZrO_3$, or alternatively $(Ba.Sr)TiO_3$ or $SrTiO_3$ or $Ca_2Nb_2O_7$ or Ta_4O_5, if appropriate doped in a suitable manner, for example with Cr For example, the dielectric layer may be formed as described in A. Beck et al., *Reproducible Switching Effect in Thin Oxide Films for Memory Applications*, Applied Physics Letters, Volume 77, p. 139, 2000, which is incorporated by reference herein in their entirety.

~~In this case the layer may contain $SrZrO_3$, or alternatively $(Ba.Sr)TiO_3$ or $SrTiO_3$ or $Ca_2Nb_2O_7$ or Ta_4O_5, if appropriate doped in a suitable manner, for example with Cr. The explanations in [5] with regard to the chemical composition of the layer, the electrode formation and linking and also the operation of the layer shall be disclosed herewith as being associated with the invention.~~

[0055] The layer may also be formed as a polymer~~.~~, as is known in the art. The layer may include a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex or chalcogenide material. For example, the polymer layer may be formed as described in H.J. Gao et al., *Reversible, Nanometer-Scale Conductance Transitions in an Organic ...*", Physical Review Letters, Volume 84, No. 8, p. 1780, 2000; and G. Wicker et al., *Nonvolatile, High Density, High Performance Phase Change Memory*, www.Ovonyx.com, both of which are incorporated by reference herein in their entirety.

~~The layer then preferably contains a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex. The explanations in [6] with regard to the chemical composition of the layer, the electrode formation and linking and also the operation of the layer shall be disclosed herewith as being associated with the invention.~~

~~However, the layer may in particular also contain chalcogenide material. The explanations in [4] with regard to the chemical composition of the layer, the electrode formation and linking and also the operation of the layer shall be disclosed herewith as being associated with the invention.~~

[0056] In order to produce an integrated read-only memory, firstly an array of selection transistors is produced using CMOS-compatible technology. Drain contacts of the selection transistors are led to the surface of the arrangement before a layer whose electrical resistance can be changed through the effect of a configuration voltage or a configuration current is deposited above the selection transistors. Finally, an electrode is arranged above the layer.

[0057] Consequently, a large-scale integrated memory can be produced in a simple manner.

[0058] In particular with a common layer for a plurality or all of the memory cells, said layer may be deposited in just one production step.

[0059] In this case, the selection transistors may be produced in a front end process and the layer may be deposited in a back end process. In this case, back end process is understood to be the chronologically last fabrication stages in semiconductor fabrication, in particular the fabrication stages after the construction of structures in the substrate.

[0060] In this case, the integration of the switchable layer in the back end process affords significant advantages in particular for organic compounds, since the switchable layer is not exposed to the temperatures in the region of up to 1000 Celsius that are customary in the front end process. Furthermore, the use of an unpatterned top electrode avoids possible damage to the electrically switchable layer by one of the patterning techniques.

[0061] The selection transistors may be constructed in planar fashion in the substrate, or alternatively vertically. In the case of planar orientation it is possible to use standard processes for production.

[0062] With regard to the layer materials and their particular features and advantages, reference is made to the explanations concerning the integrated read-only memory.

~~Exemplary embodiments of the invention are illustrated in the figures and are explained in more detail below.~~

~~In the Figures:~~

~~Figure 1 shows a cross section through part of an integrated read-only memory in accordance with a first exemplary embodiment of the invention using planar selection transistors;~~

~~Figure 2 shows a cross section through part of an integrated read-only memory in accordance with a first exemplary embodiment of the invention using vertical selection transistors; and~~

~~Figure 3 shows a perspective view with elements illustrated partly in exploded fashion in a detail from a read-only memory according to Figure 2.~~

~~Identical elements are identified by the same reference symbols throughout the figures.~~

[0063] Figure 1 shows a cross section through part of an integrated read-only memory in accordance with a first exemplary embodiment of the invention.

[0064] In this case, the read-only memory contains an n-channel MOSFET as selection transistor 15. In this case, an N-type drain region 11 and an N-type source region 12 are created by doping in a p-type substrate. A gate 5 with a polysilicon gate 8 and also a tungsten layer 7 and a nitride layer 6 thereabove is applied, in a manner insulated by an oxide layer 9 above the channel between drain region 11 and source region 12.

[0065] Oxide spacers 10 insulate the gate 5 laterally from a source connection 4, predominantly produced from polysilicon, and also a drain connection 3, which is led upward as a metallic plug.

[0066] Source connection 4 and drain connection 3 make contact with the source region 12 and the drain region 11, respectively, in the substrate 13.

[0067] At the other end, the source connection 4 is connected to a bit line 14. For its part, the drain connection 3 is connected to an electrically switchable layer 2, for example a rotaxane molecular layer, which, for its part, is covered by an electrode 1.

[0068] Further selection transistors adjoin on both sides of the planar selection transistor 15. Thus, by way of example, a further drain connection of a selection transistor is shown on the right-hand side, which is likewise connected to the layer 2.

[0069] The arrangement according to Figure 1 therefore only shows a detail from an array of memory cells of a read-only memory, in particular only a marked memory cell with a selection transistor 15 and an associated section – around the drain connection 3 – of the layer 2 as memory element which can be locally configured in this region.

[0070] In particular, the resistance of the layer 2 can in this case be changed locally through the effect of a voltage present at the electrode 1. Consequently, the local electrical behavior of the layer 2 can be set once or repeatedly depending on the chemical composition of the layer material by means of voltage or current pulses. The totality of this electrically switchable layer constitutes the actual memory elements which are represented by local regions in the layer with different resistance characteristic values. In particular, it can be discerned that the drain connections 3 of a plurality of selection transistors are connected to this common layer 2, and, consequently, a single layer that can be differently configured locally in terms of its electrical properties holds all the memory contents ready.

[0071] The gate 5 is connected to a word line (not depicted). In order to read out the content of the memory cell represented, the gate 5 is activated via the word line. A predetermined read voltage is present at the electrode. The memory content is tapped off at the bit line during the gate driving. If the rotaxane layer 2 is programmed as an open switch, then in the case of a read voltage which effects a negative polarity in the layer, the layer 2 permits a current flow that is detected on the bit line. However, if the rotaxane layer is

programmed as a closed switch, i.e. a positive voltage of greater than 0.7 Volt has already been applied to the electrode, then the rotaxane layer 2, on account of its molecular state, no longer permits a current flow, this likewise being detected on the bit line.

[0072] During the production of such an integrated read-only memory, first the selection transistors are created in standard CMOS processes. After preparation of the source and drain connections 4 and 3, the electrically switchable layer 2 is applied in the back end process, before said layer 2 is covered with the electrode 1.

[0073] Figure 2 shows a cross section through part of an integrated read-only memory in accordance with a second exemplary embodiment of the invention.

[0074] In contrast to the exemplary embodiment according to Figure 1, the selection transistors 15 are now arranged vertically in the substrate 13.

[0075] An N-type source region 12, a P-type region 16 and an N-type drain region 11 are arranged one above the other. On lateral vertical oxide layers 9, vertical gates 5 made of polysilicon are arranged on both sides of the above-described stack. Oxide spacers 10 are provided for insulation purposes between the gates 5 of adjacent vertical selection transistors 15.

[0076] The N-type drain regions 11 are again connected to the electrically switchable layer 2 that has already been described in more detail in connection with Figure 1, the electrode 1 again being applied on said layer.

[0077] The N-type source regions are again connected to bit lines 14 arranged below the selection transistors 15.

[0078] The word lines connected to the gates 5 are again not depicted.

[0079] The layer 2 is applied to the vertical transistor arrangements according to Figure 2 in the back end process.

[0080] Figure 3 shows a detail from an integrated read-only memory according to Figure 2, in the picture only with a single vertical selection transistor 15, in an exploded illustration.

[0081] In this case, layer 2 and electrode 1 are lifted off in exploded fashion from the single selection transistor 15.

[0082] In particular, it is possible to see the structure and arrangement of bit lines 14 that are mutually insulated among one another by oxide spacers 10.

The following publications are cited in this document:

[1] C.P. Collier et al., Electronically Configurable Molecular Based Logic Gates, Science, Volume 285, p. 391, 1999

[2] C.P. Collier et al., A [2]Catenane Based Solid State Electronically Reconfigurable Switch, Science, Volume 289, p. 1172, 2000

[3] D.I. Gittins et al., A Nanometre Scale Electronic Switch Consisting of a Metal Cluster and Redox Addressable Groups, Nature, Volume 408, p. 67, 2000

[4] G. Wicker et al., Nonvolatile, High Density, High Performance Phase Change Memory, www.Ovonyx.com

[5] A. Beck et al., Reproducible Switching Effect in Thin Oxide Films for Memory Applications, Applied Physics Letters, Volume 77, p. 139, 2000

[6] H.J. Gao et al., Reversible, Nanometer Scale Conductance Transitions in an Organic ...", Physical Review Letters, Volume 84, No. 8, p. 1780, 2000

[7] US 4,590,589

~~List of reference symbols~~

~~1 Electrode~~

~~2 Layer~~

~~3 Drain connection~~

~~4 Source connection~~

~~5 Gate~~

~~6 Nitride layer~~

~~7 Tungsten layer~~

~~8 Polysilicon gate~~

~~9 Oxide layer~~

~~10 Oxide spacer~~

~~11 N-type drain region~~

~~12 N-type source region~~

~~13 P-type substrate~~

~~14 Bit line~~

~~15 Selection transistor~~

~~16 P-type region~~

~~Patent c~~Claims

1. An integrated read-only memory, comprising

~~having~~ a plurality of selection transistors each having a drain connection,

~~having~~ an electrode for feeding a voltage or a current~~;~~;

~~having~~ a layer between ~~the~~ each drain connections and the electrode, having a modifiable ~~the~~ electrical resistance ~~of which can be changed~~ through ~~the effect of~~ a configuration ~~voltage or a configuration current~~electrical signal,

~~having~~ a source connection per selection transistor~~;~~;

~~having~~ a bit line that is electrically connected to at least one source connection~~;~~;

~~in which~~ where the layer is formed as a common layer for linking the drain connections to the electrode, and

~~in which~~ where the electrical resistance of the layer can be changed locally.

2. The read-only memory ~~as claimed in~~ of claim 1, ~~in which~~ where the resistance of the layer can be switched over.

3. The read-only memory ~~as claimed in~~ of claim 1 ~~or 2, in which~~ where the resistance of the layer can be switched over between ~~two~~ multiple resistance characteristic curves.

4. The read-only memory ~~as claimed in one of the preceding~~ of claims 1, comprising:

~~having~~ a read ~~voltage~~ signal applied to the layer ~~or a read current fed to the layer~~ within a defined ~~voltage or current~~ signal range in a read operation of the read-only memory, and

~~having~~ a configuration ~~voltage or a configuration current~~ signal outside the ~~voltage or current~~ read signal range ~~provided for the read operation~~ in a configuration operation of the read-only memory.

5. The read-only memory ~~as claimed in one of the preceding~~ of claim 1s, ~~which~~ where the read-only memoryis ~~designed as~~ a flash memory.

6. The read-only memory ~~as claimed in one of the preceding~~ of claims 1, ~~in which~~ where the selection transistors are arranged in an array.

7. The read-only memory ~~as claimed in one~~ of claims ~~1 to 6~~, ~~in which~~ where the bit line is connected to a decoder circuit.

8. The read-only memory ~~as claimed in one~~ of claims 1 ~~to 7~~, ~~in which~~ where the bit line is accessible for an external connection.

9. The read-only memory ~~as claimed in one of the preceding~~ of claims 1, comprising:

~~having~~ a gate connection per selection transistor~~;~~; and

~~having~~ a word line ~~that is~~ being electrically connected to at least one gate connection.

10. The read-only ~~memory as claimed in~~ of claim 9, ~~in which~~ where the word line is connected to a decoder circuit.

11. The read-only memory ~~as claimed in~~ of claim 9 ~~or claim 10~~, ~~in which~~ where the word line is accessible for an external connection.

12. The read-only memory ~~as claimed in one of the preceding~~ of claims 9, ~~in which~~ where the selection transistors have a substantially planar construction in the substrate.

13. The read-only memory ~~as claimed in one of~~ of claims ~~1 to 11~~, ~~in which~~ where the selection transistors have a vertical construction in the substrate.

14. The read-only memory ~~as claimed in one of the preceding~~ of claims 1, ~~in which~~ where the layer is formed as a molecular layer.

15. The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ where the layer contains rotaxane.

16. The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ where the layer contains catenane.

17. The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ where the layer contains a bispyridinium compound.

18. The read-only memory ~~as claimed in one~~ of claims ~~1 to 13~~, ~~in which~~ where the layer is formed as a dielectric.

19. The read-only memory ~~as claimed in~~ of claim 18, ~~in which~~ where the layer contains $SrZrO_3$.

20. The read-only memory ~~as claimed in one~~ of claims 1 ~~to 13~~, ~~in which~~ where the layer is formed as a polymer.

21. The read-only memory ~~as claimed in~~ of claim 20, ~~in which~~ where the layer contains 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

22. The read-only memory ~~as claimed in~~ of claim 20, ~~in which~~ where the layer contains a chalcogenide compound.

23. A method for operating an integrated read-only memory having a plurality of selection transistors each having a drain connection and an electrode for feeding a voltage or a current, including a layer between each drain connection and the electrode, ~~as claimed in one of the preceding claims~~, comprising:

providing a layer between each drain connection and the electrode, they layer having a modifiable electrical resistance through a configuration electrical signal, where the layer is formed as a common layer for linking the drain connections to the electrode, and where the electrical resistance of the layer can be changed locally;

applying ~~in which~~ in a read operation, a read voltage or a read current within a defined voltage or current range is applied to the layer~~,~~; and

applying ~~in which,~~ in a configuration operation, a configuration voltage or a configuration current outside the voltage or current range provided for the read operation is applied to the layer.

24. A method for producing an integrated read-only memory, comprising:

~~in which~~ producing an array of selection transistors ~~is produced~~ using CMOS technology~~;~~;

~~in which~~ leading drain contacts of the selection transistors ~~are led~~ to the surface of the arrangement~~;~~;

~~in which~~ depositing a layer ~~is deposited whose~~ having an electrical resistance that can be changed through the effect of a configuration ~~voltage or a configuration current~~signal, ~~it being possible for~~ where the electrical resistance of the layer ~~to~~ may be changed locally~~;~~;

~~in which~~ arranging an electrode is arranged above the layer~~;~~;

~~in which~~ forming a source connection ~~is formed~~ per selection transistor~~;~~;

~~in which~~ forming a bit line ~~is formed~~ which is electrically connected to at least one source connection~~;~~; and

~~in which~~ forming the layer ~~is formed~~ as a common layer for linking the drain connections to the electrode.

25. The method for producing an integrated read-only memory ~~as claimed in~~ of claim 24, ~~in which~~ where the layer is deposited as a common layer for linking the drain connections to the electrode above the selection transistors.

26. The method for producing an integrated read-only memory ~~as claimed in~~ of claim 24 ~~or claim 25~~, ~~in which~~ where the selection transistors are produced in a front end process.

27. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 26~~, ~~in which~~ where the layer is deposited in a back end process.

28. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 27~~, ~~in which~~ where the selection transistors are constructed in substantially planar fashion in the substrate.

29. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 27~~, ~~in which~~ where the selection transistors are constructed vertically in the substrate.

30. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ where the layer is formed as a molecular layer.

31. The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ where the layer contains rotaxane.

32. The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ where the layer contains catenane.

33. The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ where the layer contains a bispyridinium compound.

34. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ where the layer is formed as a dielectric.

35. The method for producing an integrated read-only memory ~~as claimed in~~ of claim 34, ~~in which~~ where the layer contains $SrZrO_3$.

36. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ where the layer is formed as a polymer.

37. The method for producing an integrated read-only memory ~~as claimed~~ of ~~in~~ claim 36, ~~in which~~ where the layer contains a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

38. The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ where the layer contains a chalcogenide compound.

ABSTRACT

An integrated read-only memory having select transistors, each of which has a drain connection and an electrode connection for feeding an electrical signal such as a voltage or a current. A layer is provided between the drain connections and the electrode, whose electric resistance can be changed under the effect of a configuration voltage or current. The layer may be applied in a backend process.